In the Claims:

Please cancel claims 15 and 25. Please amend claims 1, 5-7, 9, 13-14, 18-19, and 26-30. Please add new claims 31-32. The claims are as follows.

1. (Currently amended) A processor, comprising M independent vector register files, said M vector register files adapted to collectively store a matrix of L data elements, each data element having B binary bits, said matrix having N rows and M columns, said L=N*M, each column having K subcolumns, said N≥2, said M≥2, said K≥[[1]]2 , said N=K.*M, said B≥1, each row of said N rows being addressable, each subcolumn of said K subcolumns being addressable, said processor not adapted to duplicatively store said L data elements.

2. (Original) The processor of claim 1, wherein the processor further comprises M address registers, wherein each address register of the M address registers is associated with a corresponding one of the M vector register files, wherein each of the M vector register files includes an array of N registers, wherein each of the N*M registers of the M vector register files are adapted to store a data element of the L data elements, and wherein each vector register file is independently addressable through its associated address register being adapted to point to one of the N registers of said vector register file.

3. (Original) The processor of claim 2, wherein the data elements of each subcolumn are adapted to be stored in different vector register files, and wherein the data elements of each row are adapted to be stored in different vector register files.

4. (Original) The processor of claim 3, wherein the data elements of each subcolumn are adapted to be stored in different relative register locations of the different vector register files, and wherein the data elements of each row are adapted to be stored in a same relative register location of the different vector register files.

5. (Currently amended) The processor of claim 3, wherein the processor further comprises M multiplexors respectively coupled to the M vector register files, wherein each multiplexor of the M multiplexors comprises a set of binary switches subject to each binary switch being on or off and respectively represented by a binary bit 1 or 0 such that the value of the multiplexor consists of the composite value of said binary bits, and wherein if the matrix is stored in the M vector register files then:

the M multiplexors are adapted to respond to a command to read a row of the matrix by mapping the data elements of the row from the M vector register files to the row of the matrix in accordance with a read-row mapping algorithm; and

the M multiplexors are adapted to respond to a command to read a subcolumn of the matrix by reading the data elements of the subcolumn from the M vector register files to the subcolumn of the matrix in accordance with a read-subcolumn mapping algorithm.

6. (Currently amended) The processor of claim 3,

wherein the processor further comprises M multiplexors respectively coupled to the M vector register files;

wherein each multiplexor of the M multiplexors comprises a set of binary switches

subject to each binary switch being on or off and respectively represented by a binary bit 1 or 0 such that the value of the multiplexor consists of the composite value of said binary bits;

wherein the M multiplexors are adapted to respond to a command to write a row of the matrix by mapping the data elements of the row to the M vector register files in accordance with a write-row mapping algorithm; and

wherein the M multiplexors are adapted to respond to a command to write a subcolumn of the matrix by mapping the data elements of the subcolumn to the M vector register files in accordance with a write-subcolumn mapping algorithm.

7. (Currently amended) The processor of claim 2, wherein the processor further comprises M multiplexors respectively coupled to the M vector register files such that each of the M multiplexors has a different value, and wherein each multiplexor of the M multiplexors comprises a set of binary switches subject to each binary switch being on or off and respectively represented by a binary bit 1 or 0 such that the value of the multiplexor consists of the composite value of said binary bits.

8. (Original) The processor of claim 1, wherein the matrix of L data elements are stored in the M vector register files.

9. (Currently amended) A method ~~for processing matrix data~~, comprising:

providing ~~the~~ a processor; ~~and~~

providing M independent vector register files within the processor, said M vector register files collectively storing a matrix of L data elements, each data element having B binary bits, said

matrix having N rows and M columns, said L=N*M, said N=K*M, each column having K subcolumns, said N≥2, said M≥2, said K≥[[1]]2 , said N=K*M, said B≥1, each row of said N rows being addressable, each subcolumn of said K subcolumns being addressable, said processor not duplicatively storing said L data elements; and

respectively coupling M multiplexors coupled to the M vector register files such that each of the M multiplexors has a different value, wherein each multiplexor of the M multiplexors comprises a set of binary switches subject to each binary switch being on or off and respectively represented by a binary bit 1 or 0 such that the value of the multiplexor consists of the composite value of said binary bits.

10. (Original) The method of claim 9, wherein the method further comprises providing M address registers within the processor, wherein each address register of the M address registers is associated with a corresponding one of the M vector register files, wherein each of the M vector register files includes an array of N registers, wherein each of the N*M registers of the M vector register files stores a data element of the L data elements, and wherein each vector register file is independently addressable through its associated address register being adapted to point to one of the N registers of said vector register file.

11. (Original) The method of claim 10, wherein the data elements of each subcolumn are stored in different vector register files, and wherein the data elements of each row are stored in different vector register files.

12. (Original) The method of claim 11, wherein the data elements of each subcolumn are stored in different relative register locations of the different vector register files, and wherein the data elements of each row are stored in a same relative register location of the different vector register files.

13. (Currently amended) The method of claim 11, wherein the method further comprises providing M multiplexors respectively coupled to the M vector register files, wherein each multiplexor of the M multiplexors comprises a set of binary switches subject to each binary switch being on or off and respectively represented by a binary bit 1 or 0 such that the value of the multiplexor consists of the composite value of said binary bits, and wherein if the matrix is stored in the M vector register files then:

the M multiplexors are adapted to respond to a command to read a row of the matrix by mapping the data elements of the row from the M vector register files to the row of the matrix in accordance with a read-row mapping algorithm; and

the M multiplexors are adapted to respond to a command to read a subcolumn of the matrix by reading the data elements of the subcolumn from the M vector register files to the subcolumn of the matrix in accordance with a read-subcolumn mapping algorithm.

14. (Currently amended) The method of claim 11,

wherein the method further comprises providing M multiplexors respectively coupled to the M vector register files;

wherein each multiplexor of the M multiplexors comprises a set of binary switches

subject to each binary switch being on or off and respectively represented by a binary bit 1 or 0 such that the value of the multiplexor consists of the composite value of said binary bits;

wherein the M multiplexors are adapted to respond to a command to write a row of the matrix by mapping the data elements of the row to the M vector register files in accordance with a write-row mapping algorithm; and

wherein the M multiplexors are adapted to respond to a command to write a subcolumn of the matrix by mapping the data elements of the subcolumn to the M vector register files in accordance with a write-subcolumn mapping algorithm.

15. (Canceled)

16. (Original) The method of claim 9, further comprising addressing a row of the N rows.

17. (Original) The method of claim 9, further comprising addressing a subcolumn of the K*M subcolumns.

18. (Currently amended) A processor, comprising M independent vector register files, said M vector register files adapted to collectively store a matrix of L data elements, each data element having B binary bits, said matrix having N rows and M columns, said L=N*M, each column having K subcolumns, said N≥2, said M≥2, said K≥[[1]]2, said N=K*M, said B≥1, each row of said N rows being addressable, each subcolumn of said K subcolumns being addressable, said matrix including a set of arrays such that each array is a row or subcolumn of the matrix, said

processor adapted to execute an instruction that performs an operation on a first array of the set of arrays, said operation being performed with selectivity with respect to the data elements of the first array.

19. (Currently amended) The processor of claim 18, wherein the processor further comprises M multiplexors respectively coupled to the M vector register files, wherein each multiplexor of the M multiplexors comprises a set of binary switches subject to each binary switch being on or off and respectively represented by a binary bit 1 or 0 such that the value of the multiplexor consists of the composite value of said binary bits, and wherein the values associated with the M multiplexors control said selectivity.

20. (Original) The processor of claim 18, wherein the processor further comprises M address registers, wherein each address register of the M address registers is associated with a corresponding one of the M vector register files, wherein each of the M vector register files includes an array of N registers, wherein each of the N*M registers of the M vector register files are adapted to store a data element of the L data elements, and wherein each vector register file is independently addressable through its associated address register being adapted to point to one of the N registers of said vector register file.

21. (Original) The processor of claim 18, wherein the instruction is adapted to copy at least one data element of the first array of the set of arrays to a second array of the set of arrays, and wherein the instruction does not insert an exact copy of the first array into the second array.

22. (Original) The processor of claim 18, wherein the instruction is adapted to rearrange the data elements of the first array within the first array.

23. (Original) The processor of claim 18, wherein the processor is not adapted to duplicatively store the L data elements.

24. (Original) The processor of claim 18, wherein the matrix of L data elements are stored in the M vector register files.

25. (Canceled)

26. (Currently amended) ~~The method of claim 25, further comprising~~ A method for processing matrix data, comprising:

providing the processor;

providing M independent vector register files within the processor, said M vector register files collectively storing a matrix of L data elements, each data element having B binary bits, said matrix having N rows and M columns, said L=N*M, each column having K subcolumns, said N≥2, said M≥2, said K≥1, said B≥1, each row of said N rows being addressable, each subcolumn of said K subcolumns being addressable, said matrix including a set of arrays such that each array is a row or subcolumn of the matrix; and

executing an instruction by said processor, said instruction performing an operation on a first array of the set of arrays, said operation being performed with selectivity with respect to the

data elements of the first array; and

providing M multiplexors respectively coupled to the M vector register files, wherein the values associated with the M multiplexors control said selectivity.

27. (Currently amended) The method of claim ~~25~~ 26, wherein the method further comprises providing M address registers within the processor, wherein each address register of the M address registers is associated with a corresponding one of the M vector register files, wherein each of the M vector register files includes an array of N registers, wherein each of the N*M registers of the M vector register files stores a data element of the L data elements, and wherein each vector register file is independently addressable through its associated address register being adapted to point to one of the N registers of said vector register file.

28. (Currently amended) The method of claim ~~25~~ 26, wherein said performing an operation includes copying at least one data element of the first array of the set of arrays to a second array of the set of arrays, and wherein said copying does not insert an exact copy of the first array into the second array.

29. (Currently amended) The method of claim ~~25~~ 26, wherein said performing an operation includes rearranging the data elements of the first array within the first array.

30. (Currently amended) The method of claim ~~25~~ 26, wherein the processor is not duplicatively storing the L data elements.

31. (New) The method of claim 26, said $K \geq 2$, said $N=K*M$.

32. (New) The method of claim 26, wherein each multiplexor of the M multiplexors comprises a set of binary switches subject to each binary switch being on or off and respectively represented by a binary bit 1 or 0 such that the value of the multiplexor consists of the composite value of said binary bits.